UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,749	07/28/2003	Shih-Ming Chen	0941-0799P	4406

2292 7590 06/29/2004

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
BOOTH, RICHARD A	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/627,749	CHEN ET AL.	
	Examiner	Art Unit	
	Richard A. Booth	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *1-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of group II in the reply filed on 6/3/04 is acknowledged. The traversal is on the ground(s) that there is no serious burden placed upon the examiner. This is not found persuasive because the search for the device and the search for the process are in different classes, and such a search places a serious burden upon the examiner.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 11-15 and 17-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Huang, U.S. Patent 6,258,667.

Huang shows the invention as claimed including a gate structure for an embedded flash memory device comprising: a semiconductor silicon substrate 60 having a memory cell area and a logic circuit area; a tunnel dielectric layer 63 of silicon

oxide formed overlying the memory cell area of the semiconductor silicon substrate; a gate structure (64,65,61) formed overlying the tunnel dielectric layer of the memory cell area; a protective layer of silicon oxide 92 formed overlying the tunnel dielectric layer and the sidewall of the gate structure; an insulating spacer 1003 formed overlying the protective layer disposed overlying the sidewall of the gate structure; a silicon oxide gate dielectric layer overlying the logic circuit area of the semiconductor silicon substrate; and a polysilicon gate layer formed overlying the gate dielectric layer of the logic circuit area (see figs. 6-11 and col. 3-line 62 to col. 5-line 30).

Regarding claim 14, note that the gate structure of Huang includes a floating gate layer overlying the dielectric layer of the memory cell area, a dielectric structure overlying the floating gate layer, and a control gate layer overlying the dielectric structure.

Claims 11-15 and 17-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Pham et al., U.S. Patent 6,589,841.

Pham et al. shows the invention as claimed including a gate structure for an embedded flash memory device comprising: a semiconductor silicon substrate 62 having a memory cell area 16 and a logic circuit area 14; a tunnel dielectric layer 18 of silicon oxide formed overlying the memory cell area of the semiconductor silicon substrate; a gate structure (20,22,24) formed overlying the tunnel dielectric layer of the memory cell area; a protective layer of silicon oxide 64 formed overlying the tunnel dielectric layer and the sidewall of the gate structure; an insulating spacer 72 formed

overlying the protective layer disposed overlying the sidewall of the gate structure; a silicon oxide gate dielectric layer 18 overlying the logic circuit area of the semiconductor silicon substrate; and a polysilicon gate layer 24 formed overlying the gate dielectric layer of the logic circuit area (see figs. 1-8 and col. 1-line 33 to col. 4-line 7).

Regarding claim 14, note that the gate structure of Pham et al. includes a floating gate layer overlying the dielectric layer of the memory cell area, a dielectric structure overlying the floating gate layer, and a control gate layer overlying the dielectric structure.

Claims 11-15 and 17-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Thio et al., U.S. Patent 6,670,227.

Thio et al. shows the invention as claimed including a gate structure for an embedded flash memory device comprising: a semiconductor silicon substrate 206 having a memory cell area 202 and a logic circuit area 208; a tunnel dielectric layer 214 of silicon oxide formed overlying the memory cell area of the semiconductor silicon substrate; a gate structure (216,218,220) formed overlying the tunnel dielectric layer of the memory cell area; a protective layer of silicon oxide 242 formed overlying the tunnel dielectric layer and the sidewall of the gate structure; an insulating spacer 248 formed overlying the protective layer disposed overlying the sidewall of the gate structure; a silicon oxide gate dielectric layer 230 overlying the logic circuit area of the semiconductor silicon substrate; and a polysilicon gate layer 232 formed overlying the

gate dielectric layer of the logic circuit area (see figs. 11-16 and col. 6-line 62 to col. 7-line 57).

Regarding claim 14, note that the gate structure of Pham et al. includes a floating gate layer overlying the dielectric layer of the memory cell area, a dielectric structure overlying the floating gate layer, and a control gate layer overlying the dielectric structure.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pham et al., U.S. Patent 6,589,841.

Pham et al. is applied as above but fails to show the protective layer having a thickness of 50-500 angstroms. However, a prima facie case of obviousness is established because Pham et al. teaches the thickness of the protective layer being in a range of 20-150 angstroms (see col. 3-lines 33-35) and a range within a claimed range establishes a prima facie case of obviousness (see MPEP 2144.05).

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thio et al., U.S. Patent 6,670,227 or Huang, U.S. Patent 6,258,667.

Thio et al. and Huang are applied as above but fail to expressly disclose the protective layer having a thickness of 50-500 angstroms. Nonetheless, it would have been obvious to one of ordinary skill in the art at the time the invention was made to determine through routine experimentation the optimum thickness of the protective layer based upon a variety of factors including the desired degree of protection of the gate structure and would not lend patentability to the instant application absent the showing of unexpected results.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Richard A. Booth whose telephone number is (571) 272-1668. The examiner can normally be reached on Monday-Thursday from 7:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Richard A. Booth
Primary Examiner
Art Unit 2812

June 27, 2004